29.8 A 3GHz Switching DC-DC Converter Using Clock-Tree Charge-Recycling in 90nm CMOS with Integrated Output Filter

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Complex designs often contain voltage islands that can operate at lower supply voltages to reduce power. These circuits require multiple supply voltages, however, it is challenging to bring in and distribute several voltages on a chip. In this paper, a fully integrated DC-DC buck converter for regional power regulation is introduced. A charge-recycling scheme is used to capture some of the energy stored in the clock-tree load and feed the charge into the DC-DC converter. Furthermore, using the multi-GHz system clock for switching significantly reduces the size of the output filter components, making their integration feasible. As a proof of concept, the proposed circuit is implemented in a 1P7M2T 90nm CMOS process. It operates at 3GHz to convert an input voltage of 1.0V to an output voltage of 0.5 to 0.7V with 40 to 100mA load current.

The major drawback of using a high switching frequency is that the dynamic switching loss in the circuit is increased. *Directly* combining the clock-tree chain with the converter switching transistors and gate driver chain merges the converter switching losses with the clock-tree switching losses. Zero-voltage switching (ZVS) and clock-tree charge-recycling are used to further reduce power loss and improve conversion efficiency. A delay circuit implemented inside the clock-tree chain provides the dead-time needed to implement ZVS. To adjust and regulate output voltage, the duty-cycle of the clock signal is changed by a control circuit. Therefore, this clock signal is intended for circuit blocks that are insensitive to clock duty-cycle, such as edge-triggered flip-flops.

The idea of using an inductor inside a clock distribution network was previously used in [1], in which a clock resonance scheme reduces power loss in the clock network. In comparison, we use charge recycling and ZVS to decrease clock power loss.

Figure 29.8.1 shows the block diagram of two implemented systems: a typical clock-tree network and our converter. A chain of cascaded inverters is used as a clock buffer. C_{clk} represents the clock network capacitance. When the clock is high, C_{clk} is charged through M_p. In the other half of the clock cycle, C_{clk} would normally be discharged to ground through M_n, wasting the stored charge. Instead, M_p and M_n can be considered as the power transistors of a switching buck converter and recycle the clock-tree charge to the output filter and consequently to the load.

The combined power and clock circuit are shown in Fig. 29.8.2 and an idealized timing diagram of the internal signals is shown in Fig. 29.8.3. In Fig. 29.8.3, D, T_{sw}, and T_{delay} represent clock duty-cycle, switching period (*i.e.*, clock period), and ZVS dead-time, respectively. As shown in Fig. 29.8.3, there are three modes of operation:

Mode 1 is intended to drive the load and charge C_{clk} through M_p. During this time, inductor current increases linearly since the voltage across it is constant.

Mode 2 is intended for charge recycling. Therefore, both M_n and M_p. are off. The charge that is stored in C_{clk} is moved to the output circuit through the inductor. This results in a rapid drop of V_{clk}, which is intended.

Mode 3 starts when the voltage across M_n is close to zero. At this time M_n is turned on to provide a low-resistance path for the inductor current. As a result, inductor current decreases linearly. The ZVS operation occurs when M_n is turned on while its source-drain voltage is close to zero, thereby reducing power loss.

Theoretically, if the falling inductor current crosses zero, M_n could be turned off to charge C_{clk} with the negative inductor current, hence providing ZVS operation for M_p. In practice, this would increase both output voltage ripple and inductor RMS current. The latter will cause additional power loss in the inductor resistance. By design, the minimum inductor current in this circuit is set close to zero to reduce the inductor RMS current, therefore, no ZVS operation is implemented for M_p. Since the inductor current does not stop at zero, the converter operates in continuous conduction mode (CCM).

The delay circuit for the ZVS operation of M_n is also shown in Fig. 29.8.2. To control the exact on/off timing of M_n and M_p, the single inverter buffer to those transistors is replaced with two separate inverters. To implement the delay time, as shown in Fig. 29.8.2, the gate of M_1 is connected to V_{clk} instead of the gate of M_2. Therefore, compared to V_p, the rising edge of V_n is delayed by T_{delay}, a duration which depends upon how quickly L_f drains C_{clk} and how fast M_1 turns on to raise V_n. Because of the positive-feedback configuration of M_1 and M_n, V_{clk} completes the fall to 0V quite rapidly. To prevent M_1 and M_2 from being on at the same time at the rising edge of V_m, the source of M_1 is connected to V_p instead of V_{dd}.

The control circuit of the power converter is also shown in Fig. 29.8.1. An on-chip PI controller is used to generate V_{ctrl} for the PWM circuit, which in turn changes the duty-cycle of the clock signal. Details of the PWM circuit are shown in Fig. 29.8.4. The input clock is delayed by two similar parallel delay lines. One of the lines has a fixed delay, while the delay of the other is controlled by V_{ctrl}. Combining these two delayed signals with a NAND gate results in a clock signal with controlled duty-cycle [4].

The on-chip filter components L_f and C_f are 320pH and 350pF, respectively. For the inductor, two thick metal layers of the process ($M6$ and $M7$) are used in parallel. The capacitors C_f and C_{clk} are implemented using the gate capacitance of a transistor array. In our implementation, C_{clk} is estimated to be 12pF.

As the power converter (circuit 1) is integrated within the clock network, an on-chip reference clock network (circuit 2) is also implemented. The effective efficiency (η_{eff}) is calculated using the difference in power needed to operate circuits 1 and 2 as follows:

$$\eta_{eff} = \frac{P_{out1}}{P_{in1} - P_{in2}} \times 100 \quad (1)$$

Here, P_{in1} and P_{in2} are the power dissipation of circuit 1 and 2, respectively, and P_{out1} is the output power of circuit 1. In our implementation, the circuits have independent supplies. At 3GHz, P_{in2} is measured to be 39.9mW. For an output voltage of 0.72V at 35.9mA load current (P_{out1} = 25.7mW), P_{in1} is measured to be 56.2mW and η_{eff} = 158%. The raw efficiency (η) of the integrated converter and clock network, without accounting for charge recycling, is

$$\eta = \frac{P_{out1}}{P_{in1}} \times 100 = 46\%.$$

For an output voltage of 0.52V at 101mA, η_{eff} = 80% and η = 48%.

The performance of the proposed converter is summarized in Fig. 29.8.5 together with results from recently reported data in [2] and [3] for comparison. Measured efficiency results are shown in Fig. 29.8.6. The total area of the integrated converter is 0.27mm^2. The chip micrograph is shown in Fig. 29.8.7.

Acknowledgements:
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References:
[1] S. C. Chan, K. L. Shepard and P. J. Restle, "Uniform-Phase Uniform-Amplitude Resonant-Load Global Clock Distributions," *IEEE J. Solid-State Circuits*, pp. 102–109, Jan., 2005.
[2] P. Hazucha et al., "A 233MHz 80%–87% Efficient Four-Phase DC-DC Converter Utilizing Air-Core Inductors on Package," *IEEE J. Solid-State Circuits*, pp. 838–845, Apr., 2005.
[3] S. Abedinpour, B. Bakkaloglu and S. Kiaei, "A Multi-Stage Interleaved Synchronous Buck Converter with Integrated Output Filter in a 0.18µm SiGe Process," *ISSCC Dig. Tech. Papers*, pp. 356–357, 2006.
[4] P. H. Yang and J. S. Wang, "Low-Voltage Pulsewidth Control Loops for SOC Applications," *IEEE J. Solid-State Circuits*, pp. 1348–1351, Oct., 2002.

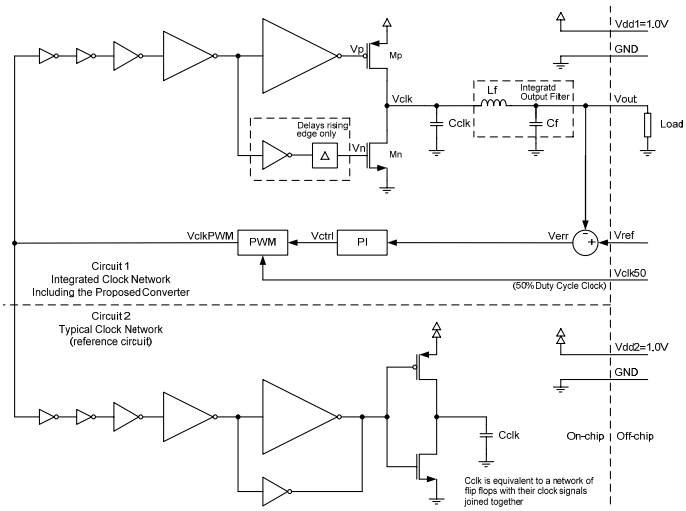

Figure 29.8.1: Block diagram of the chip.

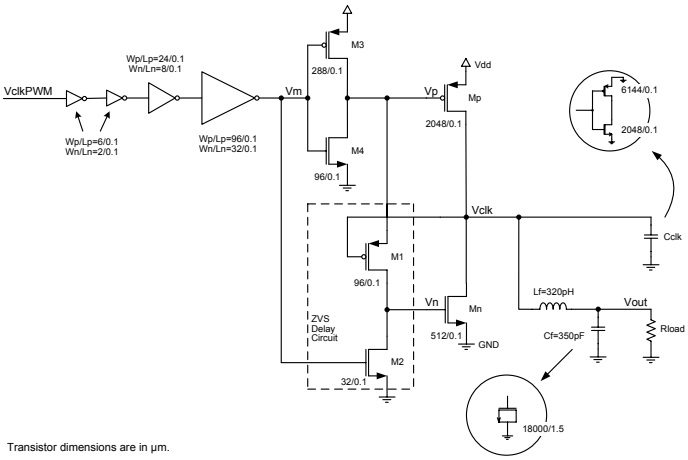

Figure 29.8.2: Circuit diagram of the integrated clock and power circuit.

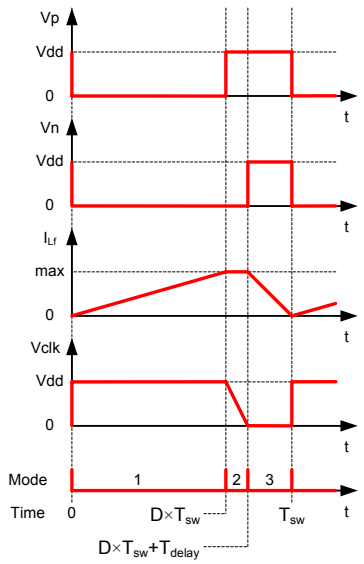

Figure 29.8.3: Idealized timing diagram of the internal signals.

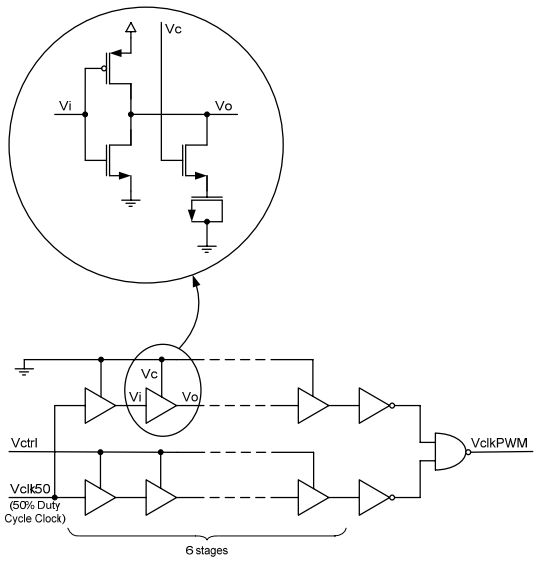

Figure 29.8.4: Details of the PWM circuit.

	This work	[2]	[3]
Year	2006	2005	2006
Converter type	Buck	4-Phase Buck	2-Phase Buck
Technology	90nm CMOS	90nm CMOS	0.18µm SiGe RFBiCMOS
Switching frequency, F_{sw} (MHz)	3000	233	45
Input voltage, V_{in} (V)	1.0	1.2 to 1.4	2.8
Output voltage range, V_{out} (V)	0.5 to 0.7	0.9 to 1.1	1.5 to 2 Nom. 1.8
Output voltage ripple (%-pp)	<5* (@ V_{out}=0.7V)		
Output current, I_{out} (mA)	40 to 100*	300 to 400	200
Effective efficiency η_{eff} (%)	158 (@ V_{out}=0.72V) 98 (@ V_{out}=0.62V) 80 (@ V_{out}=0.52V)	83.2 to 84.5	65
Filter inductor, L_f (nH)	0.32	6.8**	11
Filter capacitor, C_f (pF)	350	2500	6000
Off/on chip passive filter components	On-chip	Off-chip, in-package inductors	On-chip
Converter area (mm²)	0.27 (including L_f and C_f)	0.14 (excludes L)	27

* Design specification
** This design uses four inductors, 6.8nH each.

Figure 29.8.5: Summary of the measured performance of the converter and comparison with [2] and [3].

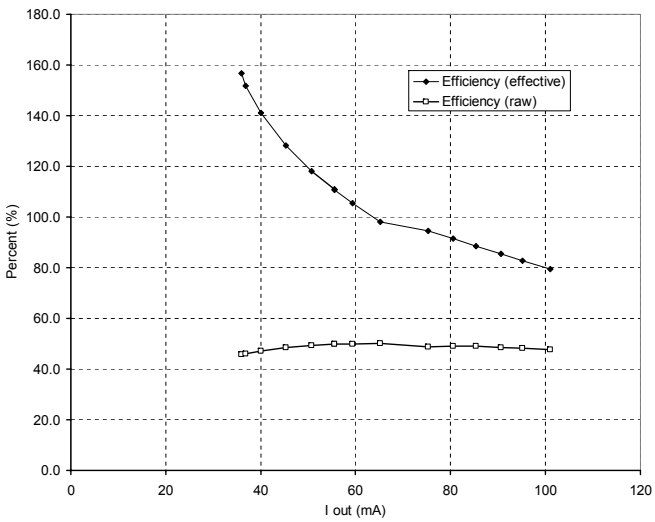

Figure 29.8.6: Measured conversion efficiency, raw and effective.

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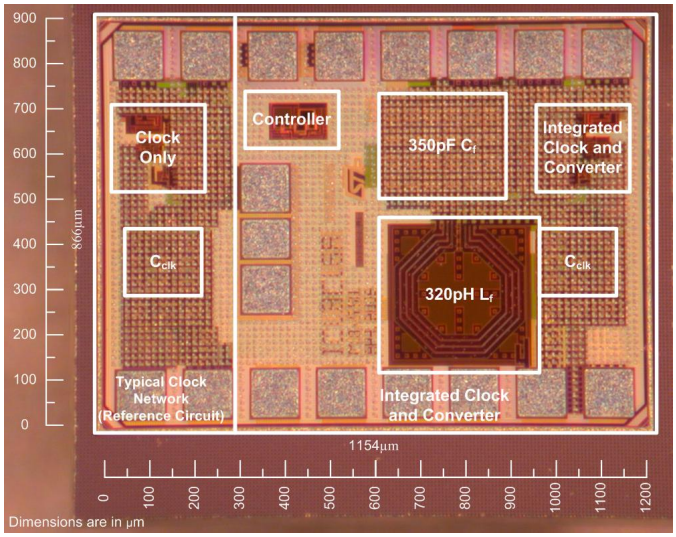

Figure 29.8.7: Chip micrograph.

